DESIGN OF HIGH SPEED MULTIPLIER USING BICMOS LOGIC FOR LARGE LOAD

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ABSTRACT

*In this paper we present a new combination of Bipolar and Cmos transistors which named BiCMOS and used to design a fast and low power circuits. New BiCMOS proposes and compare to the CMOS design. Proposed BiCMOS logic has advantages such as large load drive capabilities, low static power dissipation, fast switching and high input impedance. The multipliers are the main key structure for designing an energy efficient processor where a multiplier design decides the digital signal processors efficiency. In this paper, 4*4 unsigned Array multiplier architecture is designed by using BICMOS logic. Extensive simulation using Cadence to investigate the delay of propose multiplier. Simulation result shows that the propose BiCMOS has better performance in terms of delay and power consumption, in compared to CMOS counterpart. Furthermore the new design reduces the chip area because of using BiCMOS logic.*

Keywords

CMOS, BICMOS, Latch up.

1. INTRODUCTION

Today, CMOS technology is the dominant semiconductor technology for microprocessors, memories and application specific integrated circuits (ASICs). The main advantage of CMOS over NMOS and bipolar technology is the much smaller power dissipation. Unlike NMOS or bipolar circuits, a CMOS circuit has almost no static power dissipation. Power is only dissipated in case the circuit actually switches. This allows to integrate many more CMOS gates on an IC than in NMOS or bipolar technology, resulting in much better performance. But the signal propagation delay due to large interconnect capacitances is a major factor which limits the performance of Cmos digital integrated circuits. The system speed is ultimately limited by the current driving capability of Cmos gates that drive large capacitive loads. The problem of driving large load is traditionally solved by using specific Cmos buffer circuits with enhanced driving capabilities. But most of the buffer configurations require a significant amount of silicon area for improvement in the signal propagation delay. Another serious problem in Cmos is Latch up condition which leads to device failure. On the other hand bipolar junction transistors offer high speed, high gain, and the low output resistance which are excellent properties for high-frequency, whereas CMOS technology offers high input resistance and is excellent for constructing simple, low-power logic gates. Taking advantage of the low static power consumption of CMOS and the high current driving capability of the bipolar transistor during transients, the BiCMOS configuration can combine the "best of both worlds". In BiCMOS latch up problem is completely eliminated and when we consider fan-out BiCMOS provide better and better performance. BICMOS could be an effective way to achieve VLSI circuit with speed-power-density performance. BiCMOS combination has significant advantages to offer, such as improved switching speed and less sensitivity with respect to the load capacitance.

Section 2 describes problem in CMOS when driving large load. Section 3 gives the introduction of latch up in CMOS. Section 4 presents the minimization of latch up in proposed system. Section 5 shows the logic styles in BICMOS. Section 6 gives the multiplier architectures, designed in this paper and output waveform are generated and displayed.

2. CMOS INVERTER

Consider Cmos inverter driving another Cmos inverter. This kind of buffer is made to drive a bigger load than just a single inverter, and this has to do with speed. The problem is that a CMOS gate can drive a current proportionally to the width of its channel: so doubling the channel width, it will be able to charge a capacitor twice as fast. Because, if we double the channel width, we should also double the input capacitance of the gate, so the stage before will take twice the time to drive the gate. So you need a gate which has the minimum possible input capacitance, while having as much as driving strength as possible. This is obtained **cascading several inverters** (the most elementary CMOS gate) with increasing channel width, so that the first has the required input capacitance and the last has the required driving strength. The tradeoff now is that each inverter has also a fixed amount of latency, so you can't solve it just cascading many inverters.

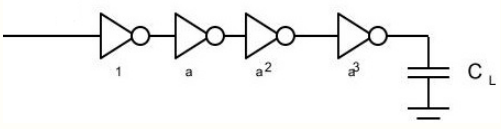

Fig. 1: Inverter chain

3. LATCHUP PROBLEM IN CMOS

Latch up is a state where a semiconductor device undergoes a high-current state as a result of interaction between a pnp and an npn bipolar transistor. The pnp and npn transistors can be natural to the technology, or parasitic devices. In CMOS technology, these are typically parasitic devices. For each p-channel MOSFET (metal oxide semiconductor field effect transistor) device, there is a corresponding parasitic pnp element formed between the p-channel diffusion, the n-well and the substrate. For each n-channel MOSFET (NMOS) device, there is a corresponding parasitic NPN element formed between the n-channel diffusion, the p_ substrate and the n-well of the p-channel MOSFET. For each inverter gate, there are corresponding pnp and npn parasitic bipolar elements. Fig.2 shows an example of a cross section of a CMOS inverter circuit.

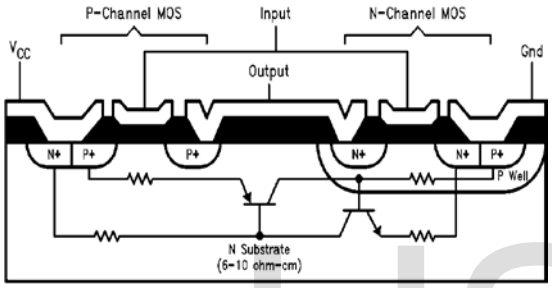

Fig.2: Basic CMOS Inverter Cross Section with Latch-Up Circuit Model

When interaction occurs between a pnp and an npn bipolar transistor, regenerative feedback between the two transistors can lead to electrical instability. This interaction between a three-region PNP and a three-region npn that share base and collector regions can be viewed as a four-region pnpn device [1–3]. As a result of the feedback between the two transistors, there exist stable and unstable regions in the I–V characteristic. When these parasitic pnpn elements undergo a high-current state, latch up can initiate thermal runaway and can be destructive [4]. Latch up events can lead to destruction of a semiconductor chip, package or system. This latch up problem is minimized by BICMOS structure.

4. MINIMIZATION OF LATCHUP IN BICMOS

How latch up is minimized by BICMOS structure? It can be done by adding retrograde n-well and epitaxial layer in an substrate. As far as MOSFET performance is concerned with low-doping substrate to achieve efficient performance. But by increasing doping concentration only latch up problem is minimized. So without degrading the MOSFET performance, a heavily doped n-well will be fabricated underneath the low doped n-well by ion implantation, this process is known as retrograde n-well and it also eliminates the subsurface punch through which normally occurs in low-doped well. Similarly by adding epitaxial layer it provide optimal MOSFET performance, so it is better technique to add both process in substrate and finally BICMOS structure arises in single substrate shown in fig:3 below. But one disadvantage is Complexity and scalability of manufacture process are major challenges of BiCMOS circuits.

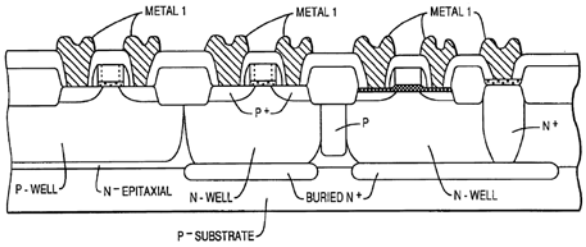

Fig.3: BICMOS structure

5. BICMOS LOGIC STYLES

BiCMOS inverter circuit is shown in Fig 3. When VIN is equal to zero then M1 transistor is turn ON then both M2 and M3 transistors are OFF. Turn ON the M1 and turn OFF the M3 provide Q1 base Current and turn it ON. In the other side turning OFF the M2, makes no current reaches to Q2 Base, at the same time the M4 can discharge the electron charges in the Q2 base in a very short time.

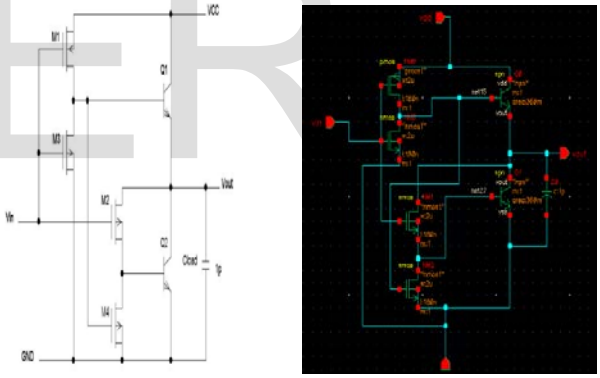

Fig. 4: Schematic diagram of conventional BiCMOS inverter

Therefore, great current (IEQ1) completely charge Cload capacitor. The gate delay propagation from low to high voltage will be low. When Vin is equal to Vcc, the M is turn OFF then both M2 and M3 are on. Turning ON the M3 makes the voltage Gate of M4 being equal to zero therefore it will be OFF. High voltage of Vout and turning ON the M2 then turning OFF the M4 supply the current base of the Q2 and turn it ON. Finally, Cload capacitor via the Q2 transistor and great current (ICQ2) can be discharged quickly.Simliarly the and, or, and, xor BICMOS logics are shown below in figures 5,6 and 7 .

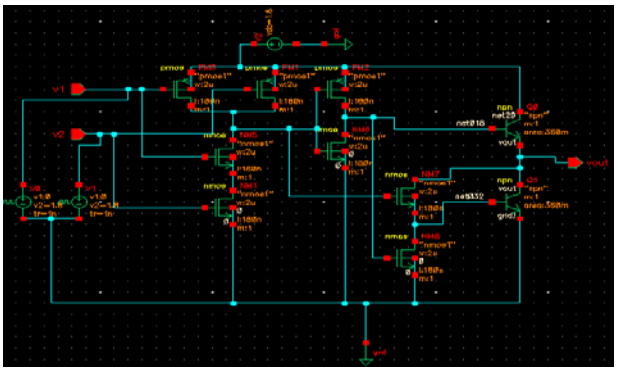

Fig.5: BICMOS AND logic

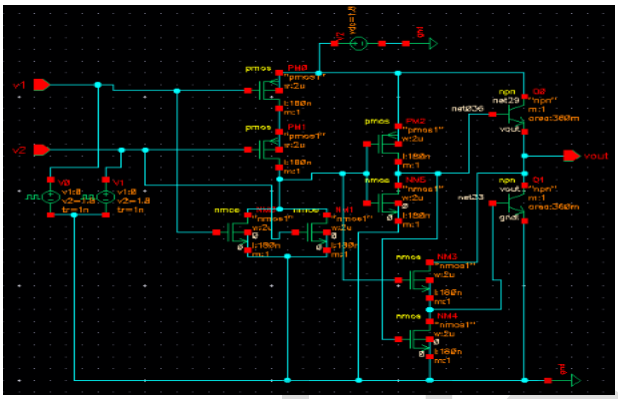

Fig.6: BICMOS OR logic

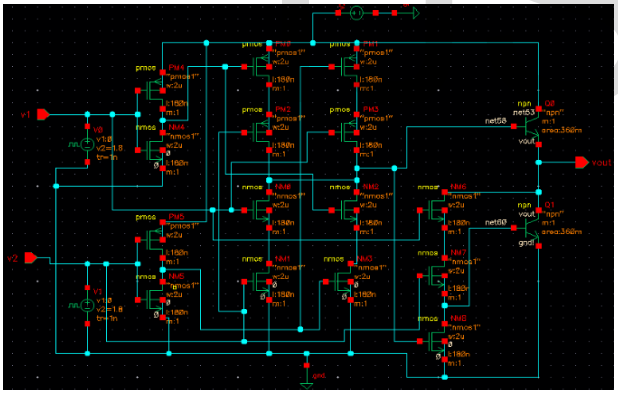

Fig.7: BICMOS XOR logic

6. MULTIPLIER ARCHITECTURE

The multipliers play a major role in arithmetic operations in digital signal processing (DSP) applications. The present development in processor designs aim at design of low power multiplier. So, the need for low power multipliers has increased. Generally the computational performance of DSP processors is affected by its multipliers performance. In this section we design 4 bit unsigned Array multiplier.

An Array multiplier [14] is very regular in structure. An n bit Array multiplier has n x n array of AND gates to generate partial products, n x (n-2) full adders and n half adders. Each partial product bit is fed into a full adder which sums the partial product bit with the sum from the previous adder and a carry from the less significant previous adder. The number of rows in array multiplier denotes length of the multiplier and width of each row denotes width of multiplicand. The output of each row of adders acts as input to the next row of adders.

Each row of full adders or 3:2 compressors adds a partial product to the partial sum, generating a new partial sum and a sequence of carries as shown in Fig.14. Schematic diagram of unsigned Array Multiplier is shown in Fig.15. In this figure (a3, a2, a1, a0) is multiplicand and (b3, b2, b1, b0) is multiplier. In place of input bit pattern voltage source is applied. P7P6P5P4P3P2P1P0 is the output of multiplier where P0 is LSB and P7 is MSB

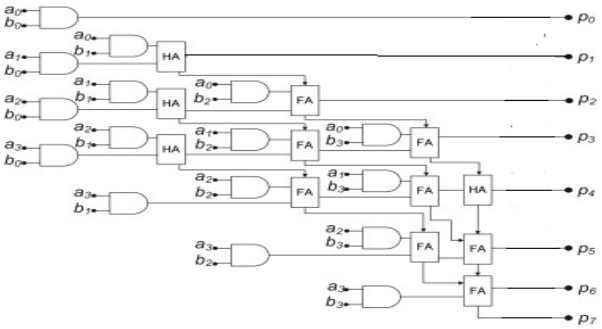

Fig.8: Schematic diagram of 4*4 unsigned Array multiplier architecture

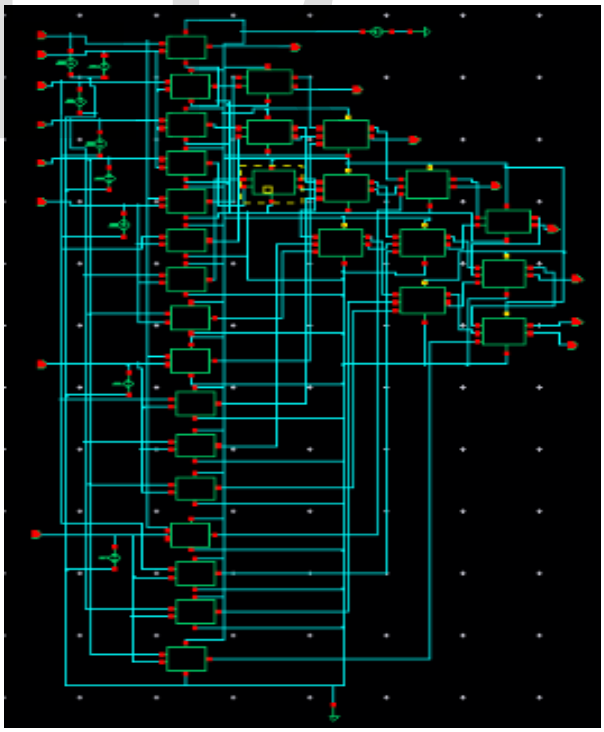

Fig.8(a): 4*4 unsigned Array multiplier architecture using BICMOS in cadence

The delay associated with the array multiplier is the time taken by the signals to propagate through the AND gates and adders that form the multiplication array. Delay of an array multiplier depends only upon the depth of the array not on the

partial product width. The delay of the array multiplier is given by [15].

T (critical) = [(N-1) + (N-2)] * T (carry) + (N-1) T (Sum) + T (AND) (3)

Where T(carry) is the propagation delay between input and output carry, T(Sum) is the delay between the input carry and sum bit of the full adder, T(AND) is the delay of AND gate, N is the length of multiplier operand. The advantage of array multiplier is its regular structure. Therefore it is easy to layout and has small size. In VLSI designs, the regular structures can be cemented over one another. This reduces the risk of mistakes and also reduces layout design time. This regular layout is widely used in VLSI math co-processors and DSP chips [16].

7.SIMULATION RESULTS AND ANALYSIS

Cadence Spectre Simulator simulates the design using with 180nm technology for BICMOS array multiplier, Simulation results are shown that a proposed BICMOS have better performance in terms of delay than the CMOS**.**The simulated waveform and its delay value is shown in fig.9 & table.1

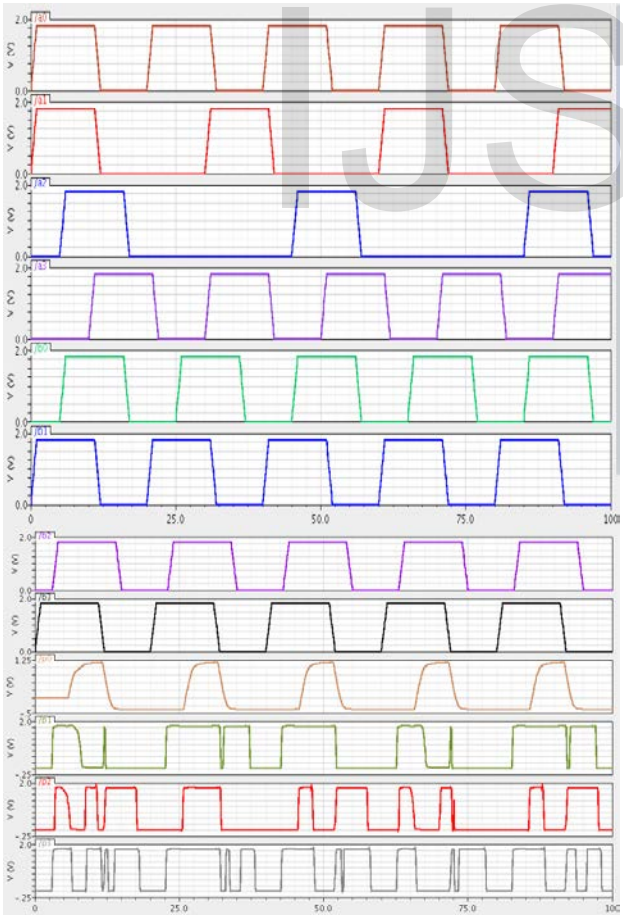

Fig.9: Simulated waveform for 4*4 unsigned Array multiplier

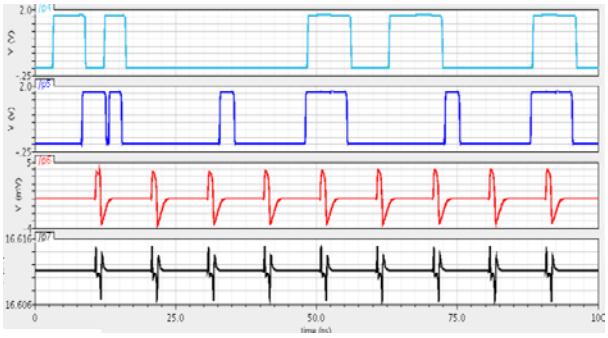

Fig.9.*Contd*. : Simulated waveform for 4*4 unsigned Array multiplier

Table.1: Delay comparison between CMOS & BICMOS

ARRAY MULTIPLIER	DELAY(ns)	
	CMOS	BICMOS
2*2	16.37	21.6
4*4	7.888	6.388

8. CONCLUSION

It has been observed that BICMOS logic exhibit better characteristics as compared to CMOS when we consider large load. So, BICMOS can be used where high speed is the prime aim.Design strategies for multiplier employing BiCMOS technology shown that low voltage, low power, and high speed application is possible.

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